I claim:

1. A memory comprising:

a plurality of banks, wherein each bank comprises

a plurality of diffused lines in a substrate and forming source/drain regions of bidirectional memory cells;

a plurality of channel regions of the bidirectional memory cells arranged in rows and columns, each of the channel regions being between a pair of the diffused lines;

a plurality of first bank select cells connected to respective pairs of the diffused lines; and

a plurality of second bank select cells connected to respective pairs of the diffused lines, wherein the pairs of diffused lines that correspond to the second bank select cells are offset relative to the pairs of diffused lines that correspond to the first bank select cells; and

a plurality of metal lines, each metal line being connected to a corresponding one of the first bank select cells and a corresponding one of the second bank select cells in each bank.

2. The memory of claim 1, further comprising a column decoding circuit coupled to bias the metal lines for an access of a selected bidirectional memory cell, wherein in response to a column address signal for the access, the column decoding circuit biases all metal lines on a first side of a selected one of the metal lines at a first voltage and biases all metal lines on a second side of the selected metal line at a second voltage.

3. The memory of claim 2, wherein:

for selection of a first storage location in the selected bidirectional memory cell, the second voltage is higher than the first voltage; and

for selection of a second storage location in the selected bidirectional memory cell, the first voltage is higher than the second voltage

4. The memory of claim 3, wherein one of the first and second voltages is ground.

5. The memory of claim 2, wherein application of the first voltage and the second voltage causes channel hot electron injection in the selected memory cell as required for programming a selected storage location in the selected bidirectional memory cell.

6. The memory of claim 1, further comprising a sense amplifier that the column decoding circuit connects to the selected metal line.

7. The memory of claim 6, wherein the column decoding circuit comprises a column decoder and a thermometer-type decoder coupled to the metal lines.

8. The memory of claim 7, wherein the column decoder controls connection of the sense amplifier to the metal lines, and the thermometer-type decoder controls connection of bias circuits to the metal lines.

9. The memory of claim 1, wherein each of the bidirectional memory cells comprises a nitride region having a first area into which channel hot electrons are injected when programming current through the bidirectional memory cell is in a first direction and a second area into which channel hot electrons are injected when programming current through the bidirectional memory cell is in a second direction.

10. The memory of claim 1, wherein each of the bidirectional memory cells comprises:

a first floating gate between the channel of the bidirectional memory cell and an overlying word line; and

a second floating gate between the channel of the bidirectional memory cell and the overlying word line, the second floating gate being laterally spaced from the first floating gate.

11. The memory of claim 1, wherein each of the bidirectional memory cells comprises two storage locations, with each of the storage locations being capable of storing a multi-bit data value that is independent of the multi-bit data value stored in the other storage location.

12. The memory of claim 1, wherein for each bank, ends of the diffused lines at a first end of the bank are all connected to the first set of bank select cells and ends of the diffused lines at a second end of the bank are all connected to the second set of bank select cells.

13. A memory comprising:

a plurality of banks, wherein each bank comprises

a plurality of diffused lines in a substrate and forming source/drain regions of bidirectional memory cells;

a plurality of channel regions of the bidirectional memory cells arranged in rows and columns, each of the channel region being between a pair of the diffused lines;

a plurality of gate insulators and insulating regions respectively overlying the plurality of channel regions, wherein the gate insulators are of a material that differs from a material in the insulating regions;

a plurality of word lines, each word line overlying the channel regions and the insulating regions of the bidirectional memory cells in a corresponding one of the rows;

a plurality of first bank select cells connected to respective pairs of the diffused lines; and

a plurality of second bank select cells connected to respective pairs of the diffused lines, wherein the pairs of diffused lines corresponding to the second bank select cells are offset relative to the pairs of diffused lines corresponding to the first bank select cells; and

a plurality of overlying lines, each overlying line being connected to a corresponding one of the first bank select cells and a corresponding one of the second bank select cells in each bank.

14. The memory of claim 13, wherein each overlying line comprise a metal line.

15. The memory of claim 13, wherein each of the bidirectional memory cells comprises two storage locations, with each of the storage locations being capable of storing a multi-bit data value that is independent of the multi-bit data value stored in the other storage location.

16. A method for accessing a selected storage location in a selected bidirectional memory cell within a memory containing a plurality of diffused lines, each diffused line forming source/drain regions for a column of bidirectional memory cells, the method comprising:

decoding a column address to identify a selected overlying line from a plurality of overlying lines and to identify a direction for a current through the selected bidirectional memory cell;

selecting a first level for a first voltage and a second level for a second voltage based on the direction for the current;

biasing all of the overlying lines that are on a first side of the selected overlying line at the first voltage and all of the overlying lines that are on a second side of the selected overlying line at the second voltage; and

activating first bank select cells that are at a first end of the bank or second bank select cells that are at a second end of the bank depending on whether the column address indicates a selected bidirectional memory cell is in an even or odd column of a selected bank, wherein each first bank select cell when activated connects a corresponding one of the overlying lines to a pair of the diffused lines, and each second bank select cell when activated connects a corresponding one of the overlying lines to a pair of the diffused lines.

17. The method of claim 16, further comprising:

decoding a row address to identify a selected word line from a plurality of word lines; and

activating the selected word line.

18. The method of claim 17, further comprising decoding the row address to identify the selected bank from a plurality of banks, wherein each of the banks includes two sets of bank select cells, and activating one of the first and second sets of bank select cells comprising activating one of the two sets of bank select cells in the selected bank.

19. A bank of a memory, comprising:

a plurality of bidirectional memory cells arranged in N columns, wherein N is greater than 2, each memory cell comprising a channel region in a substrate, a charge trapping structure overlying the channel region, and a control gate overlying the charge trapping structure;

N+1 diffused lines, wherein each of the N columns of bidirectional memory cells is between an adjacent pair of the N+1 diffused lines, portions of the adjacent pair of diffused lines forming source/drain regions of the bidirectional memory cells in the column between the adjacent pair of bit lines;

a plurality of first bank select cells, each first bank select cell comprising a transistor between a corresponding adjacent pair of the diffused lines and contact to a corresponding metal line; and

a plurality of second bank select cells, each second bank select cell comprising a transistor between a corresponding adjacent pair of the diffused lines and contact to a corresponding one of the metal lines, wherein the adjacent pairs of diffused lines corresponding to the second bank select cells are offset relative to the adjacent pairs of diffused lines corresponding to the first bank select cells.

20. The bank of claim 19, further comprising an additional first bank select cell that connects to a single one of the diffused lines that is at one edge of the bank, and an additional second bank select cell that connects to a single one of the diffused lines that is at another edge of the bank.

21. The bank of claim 19, wherein each charge trapping structure comprises a silicon nitride region adjacent to a gate oxide layer.

22. The memory of claim 19, wherein each charge trapping structure comprises an electrically conductive region that is surrounded by insulating material.

23. The memory of claim 19, wherein each of the bidirectional memory cells comprises two storage locations, with each of the storage locations being capable of storing a multi-bit data

value that is independent of the multi-bit data value stored in the other storage location.